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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,151	07/15/2003	Matthew A. Kliesner	72206	8500

27975 7590 09/29/2006

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 09/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

SF

Office Action Summary	Application No.	Applicant(s)	
	10/620,151	KLIESNER ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11-14* is/are rejected.

7)☒ Claim(s) *5,10 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/15/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4, 6-9 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Gersbach et al. U.S. Patent 5,245,637.

Regarding claim 1, referring to figure 1,

In column 4 lines 55-68, Gersbach et al. teaches that a local clock signal 14 output by the local oscillator 12 is directed to a delay element 18 which outputs a plurality n of phase-delayed signals of the same frequency as the local clock signal 14.

The plurality n of phase-delayed signals are coupled to a multiplexer 30, which extracts the phase-shifted local clock signal which most accurately represents the present phase shift between the received composite signal and the local clock signal based on (i) the second control signal output by the control logic circuit and (ii) the output of the up/down counter; see column 3 lines 20-45, also FIG. 1. Output of multiplexer 30 corresponds to the claimed output port.

Regarding claim 2, as recited in claim 1, the plurality n of phase-delayed signals are coupled to a multiplexer 30, which extracts the phase-shifted local clock signal

which most accurately represents the present phase shift between the received composite signal and the local clock signal based on (i) the second control signal output by the control logic circuit and (ii) the output of the up/down counter. Furthermore, in column 6 lines 50-65, as shown in the particular example of FIG. 3, the local clock frequency is slightly lower than that of the data clock. However, ***the local clock frequency could be slightly higher than that of the data clock***. In either case, the principles of the present invention may be applied to compensate for this frequency difference.

Regarding claim 3, as recited in claim 1, the plurality n of phase-delayed signals are coupled to a multiplexer 30, which extracts the phase-shifted local clock signal which most accurately represents the present phase shift between the received composite signal and the local clock signal based on (i) the second control signal output by the control logic circuit and (ii) the output of the up/down counter. Furthermore, in column 6 lines 50-65, as shown in the particular example of FIG. 3***, the local clock frequency is slightly lower than that of the data clock***. However, the local clock frequency could be slightly higher than that of the data clock. In either case, the principles of the present invention may be applied to compensate for this frequency difference.

Regarding claim 4, in column 3 lines 20-60, Gersbach et al. teaches that by comparing the differences in frequency and phase of the received composite signal and

the local clock signal, the sampling times may be adjusted on a real time basis. Furthermore, the logic circuit 24 issues a first control signal containing frequency difference information to an up/down counter 28 and a second control signal containing phase shift information to a multiplexer; see also FIG. 1, column 3 lines 20-45. The second control signal corresponds to the claimed phase error signal.

Regarding claim 6, claim is rejected on the same ground as for claim 1 because of similar scope. Furthermore, referring back to FIG. 1, sorting circuit 20, barrel shifter 26, counters 22, control logic 24 and up/down counter 28 constitute the claimed control circuit.

Regarding claim 7, claim is rejected on the same ground as for claim 2 because of similar scope.

Regarding claim 8, claim is rejected on the same ground as for claim 3 because of similar scope.

Regarding claim 9, claim is rejected on the same ground as for claim 4 because of similar scope.

Regarding claim 11, claim is rejected on the same ground as for claim 6 because of similar scope.

Regarding claim 12, claim is rejected on the same ground as for claim 7 because of similar scope.

Regarding claim 13, claim is rejected on the same ground as for claim 8 because of similar scope.

Regarding claim 14, claim is rejected on the same ground as for claim 9 because of similar scope.

Allowable Subject Matter

2. Claims 5, 10 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jung et al. U.S. Patent 5,887,040 discloses "High Speed Digital Data Retiming Apparatus".

Song U.S. Patent 6,917,660 discloses "Adaptive De-Skew Clock Generation"

Nguyen U.S. Patent 6,285,226 B1 discloses "Duty Cycle Correction Circuit And Method".

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran

KHANH TRAN
Primary Examiner